

## Product Description

The software definable GNSS core enables simultaneous reception of all commercial GNSS signals in the 1560-1610MHz frequency range. It contains all the RF, IF, analog, data converter and power management circuitry for a complete GNSS core in a low cost CMOS 180nm process. The core includes clock generation circuitry for a configurable 2/3 bit quadrature converter which also provides a low jitter clock source for SoC applications. The configurable core can receive the traditional GPS L1 frequencies as well as the GLONASS G1, Galileo E1 and Compass B1-1 and B1-2 bands. A configurable bandpass filter and variable rate A/D converter allows each band to be received separately in single channel mode or all bands to be received together for high precision applications. The design employs a unique quadrature detection architecture for maximum flexibility.

An integrated FRAC-N synthesizer can be configured for a wide range of low cost cellular crystal frequencies from 10MHz-52MHz.

## Typical Applications

- Cellular Phones and Handheld Products
- Asset Tracking
- Precision Location and Positioning
- GNSS Timing Applications

## Features

### Single Channel Mode

- GPS L1 1575.42MHz
- GLONASS G1 1603.50MHz
- Galileo E1 1575.42MHz
- Compass B1-1 1561.098MHz
- Compass B1-2 1589.792MHz

### Block Conversion mode

- Variable sampling rate 8-80MHz
- Simultaneous conversion of all commercial GNSS signals

### Configurable 3/4 wire controller

### 2/3 bits A/D Quadrature detection

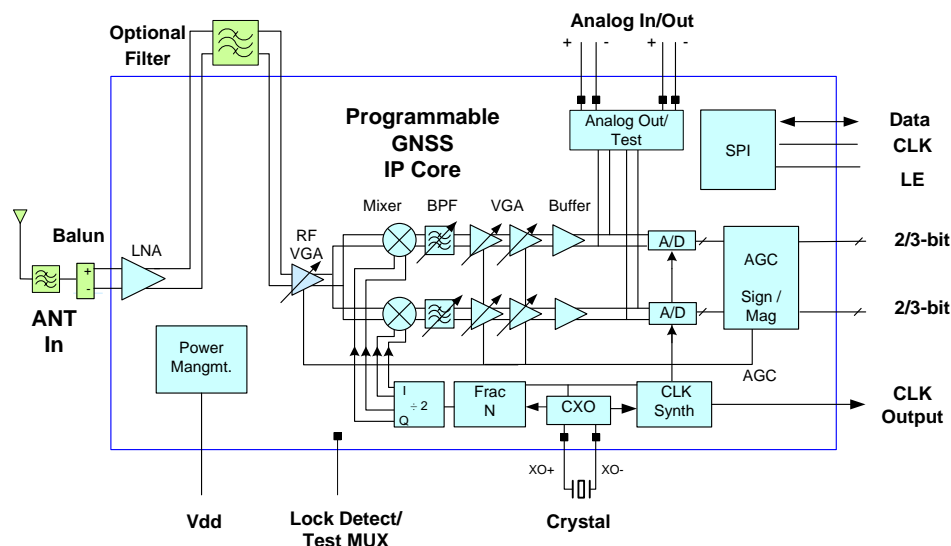
### Integrated AGC

- 50dB gain control range
- Programmable threshold

### Low Power

- Single 1.8V supply with internal regulation
- 18mA in Single Channel mode
- 29mA in Block Conversion

## Functional Block Diagram



## GNSS Core Specifications

Parameter	Conditions	Units	Min	Typ	Max
RF Frequency Range		MHz	1560		1610
IF Frequency	Configured Via SPI Interface	MHz	4		50
Sampling Rate		MHz	8		80
Band Pass Filter Bandwidth	Configured Via SPI Interface	MHz	2		44
Max Gain	LNA Enabled			100	
Max Gain	Downconverter only	dB		80	
Gain control range		dB		50	
Step size		dB		0.25	
Noise Figure	LNA Enabled	dB		2	
Noise Figure	Downconverter only	dB		10	
SSB Phase Noise	At 1kHz offset for 1.6GHz LO	dBc/Hz		-94	
SSB Phase Noise	At 10kHz offset for 1.6GHz LO	dBc/Hz		-102	
SSB Phase Noise	At 100kHz offset for 1.6GHz LO	dBc/Hz		-101	
SSB Phase Noise	At 1MHz offset for 1.6GHz LO	dBc/Hz		-124	
RMS phase error	1.5GHz LO frequency	degrees		3	
RMS Clock Jitter		ps		3	
Current	Vdd 1.8V Block conversion mode	mA		29	
Current	Vdd 1.8V Single Channel mode	mA		18	
Reference Frequency		MHz	10		52
A/D converter resolution	Configured Via SPI Interface			2/3	

### IP Status - Presilicon

### Preliminary Information

This datasheet contains information from the design target specification. RF integration Inc. reserves the right to change information at any time without notification.

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